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Matsuda et al.

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(54) **SEMICONDUCTOR DEVICE HAVING A
FERROELECTRIC TFT AND A DUMMY
ELEMENT**

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(52) **U.S. Cl.** 257/295; 257/213; 257/296

(58) **Field of Search** 257/296-310,
257/532, 213, 295

(56) **References Cited**

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(57) **ABSTRACT**

The present invention provides a semiconductor device including a semiconductor element and a dummy semiconductor element adjacent to the semiconductor element. When the semiconductor element is a capacitor element including a bottom electrode, a top electrode and a dielectric layer between the electrodes, a dummy capacitor element also has dummy electrodes and a dummy dielectric layer between the dummy electrodes. The dummy electrode is located so that a space between the top electrode of the capacitor element and the dummy top electrode is in a predetermined range (e.g. 0.3 μm to 14 μm). The dummy capacitor element prevents the capacitor dielectric layer from degrading since the collision of the etching ions with the capacitor dielectric layer in a dry etching process is suppressed.

5 Claims, 21 Drawing Sheets

